IN THE SPECIFICATION

Page 5, line 22, subsequent to "region 76" please insert - - (see FIG. 10) - - .

Page 6, line 1, subsequent to "region 93" please insert - - (see FIG. 10) - - .

Page 6, line 5, subsequent to "sloped edge" please insert - - or side surface 94 - - .

A clean copy of pages 5 and 6 with the above amendments included are immediately below for the Examiner's convenience.

Detailed Description of the Drawings

In the figures, elements having the same reference numbers have similar functionality.

FIG. 1 is a top plan view of an integrated circuit 10, showing a semiconductor substrate 11 having a top surface 32 for defining an active region 12 and a low permittivity dielectric region 14. Active region 12 is formed with active circuitry that includes transistors and/or other active components. Components of integrated circuit 10 are configured to operate at a frequency of at least six gigahertz. In one embodiment, substrate 11 is formed with silicon.

Dielectric region 14 is formed within a boundary 15 of an insulating material having a reduced permittivity structure. Hence, dielectric region 14 is ideal for forming passive components such as inductors which have a low parasitic capacitance and a high degree of electrical isolation from substrate 11, and therefore a high quality factor and frequency response. A recessed region 76 (see FIG. 10) is defined by edges 70 and 71 of a surface 73 formed on a bottom surface of substrate 11 as described

Cont'd A1

below to further enhance the quality factor of passive components formed on dielectric region 14.

A recessed region 93 (see FIG. 10) is used to align integrated circuit 10 on a die attach flag with other similarly configured semiconductor dice to provide a circuit with multiple interconnected semiconductor dice. Recessed region 93 has a sloped edge or side surface 94 defined by corners or edges 91 and 92 as described in further detail below.

A2

FIG. 2 is a top view of integrated circuit 10 showing a portion of dielectric region 14 in further detail. A dielectric material 17 is formed on substrate 11 so as to define an array of holes or cavities 16. Cavities 16 typically are filled with a gaseous material or vacuum which has a low dielectric constant, thereby reducing the effective permittivity and enhancing the frequency response of components formed on dielectric region 14. Dielectric material 17 is preferably formed to a depth of at least five micrometers in order to electrically isolate passive components from being loaded by substrate 11. In one embodiment, dielectric material 17 comprises thermally grown silicon dioxide formed to a depth of about thirty micrometers and formed in accordance with a method disclosed

in pending U.S. patent application serial number 09/527,281, filed on March 17, 2000 by the same inventor, Robert B. Davies, and entitled "Die Attachment and Method". The effective width of cavities 16 is about 1.2 micrometers and cavities 16 are